IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) An orthogonal code generating circuit for generating an orthogonal code which is defined as a code stream of ~~an~~ a Hadamard matrix constructed of $2^k x 2^k$ (symbol "k" being integer larger than, or equal to 0), comprising:

a counter circuit unit for counter-outputting code stream positional signals of said Hadamard matrix from a predetermined initial ~~phase~~ value up to a maximum value in an increment order when a code generation starting signal is entered into said counter circuit unit;

a control circuit unit for outputting a decode output based upon a code designation signal used to designate a code number of said Hadamard matrix; and

a combination circuit unit for AND-gating said ~~counter output~~ counter-output derived from said counter circuit unit and said decode output derived from said control circuit unit ~~with respect to output bits corresponding thereto~~, and ~~also~~ for exclusively OR-gating output bits generated by said ~~AND-gated output bits~~ AND-gating to thereby output serial data of said orthogonal code,

wherein said control circuit unit outputs said decode output in such a manner that since a code length designation signal for designating a code length shorter than, or equal to a maximum code length is inputted, said code designation signal is used so as to designate a code length designated based upon said code length designation signal; and

said combination circuit unit outputs said orthogonal code made based upon said code designation signal for the code length designated.

2-14. (Cancelled)